DHANALAKSHMI SRINIVASAN INSTITUTE OF TECHNOLOGY

Samayapuram – 621 112

Department of Electrical and Electronics Engineering

DEPT/YEAR/SEM/SECTION : ECE / II / III

SUBJECT TITLE : DIGITAL ELECTRONICS

INSTRUCTOR : Dr B.SUGANTHI

1.TEXT BOOKS:

1. M. Morris Mano and Michael D. Ciletti, ―Digital Design‖, 5th Edition, Pearson, 2014.

2.REFERENCES:

1. Charles H.Roth. ―Fundamentals of Logic Design‖, 6th Edition, Thomson Learning, 2013.

2. Thomas L. Floyd, ―Digital Fundamentals‖, 10th Edition, Pearson Education Inc, 2011

3. S.Salivahanan and S.Arivazhagan―Digital Electronics‖, Ist Edition, Vikas Publishing House pvt Ltd, 2012.

4. Anil K.Maini ―Digital Electronics‖, Wiley, 2014.

5. A.Anand Kumar ―Fundamentals of Digital Circuits‖, 4th Edition, PHI Learning Private Limited, 2016.

6. Soumitra Kumar Mandal ― Digital Electronics‖, McGraw Hill Education Private Limited, 2016.

3. LECTURE PLAN

SI.No	**TOPIC NAME**	**No.of. Hours**	**Books**	**Page.No**	**Teaching Kit**
UNIT-I	DIGITAL FUNDAMENTALS				
1.	Number Systems – Decimal, Binary,	1	T1,R6	12,35	BB
2.	Octal, Hexadecimal, 1_s and 2_s complements,	1	R6	50	BB
3.	Codes –Binary, BCD, Excess 3,	1	T1,R6,	25,36,50	BB
4.	Gray, Alphanumeric codes,	1	R6	60	BB
5.	Boolean theorems,	1	R6	65,	BB
6.	Logic gates, Universal gates,	1	R2	32	BB
7.	Sum of products and product of sums, Minterms and Maxterms,	1	R6	68	BB
8.	Karnaugh map Minimization	1	R6	85	BB
9.	Quine-McCluskey method of minimization.	1	R6	88,75	BB
	Total Hours 9				
UNIT II COMBINATIONAL CIRCUIT DESIGN					
10.	Design of Half and Full Adders	1	T1	102,110	BB
11.	Half and Full Subtractors	1	R2	115	BB

12.	Binary Parallel Adder	1	T1	126	BB
13.	Carry look ahead Adder,	1	T1	135	BB
14.	BCD Adder,	1	R2	142	BB
15.	Multiplexer, Demultiplexer,	1	R2	151	BB
16.	Magnitude Comparator,	1	T1	162	BB
17.	Decoder, Encoder,	1	T1	165	BB
18.	Priority Encoder.	1	T1	170	BB
	Total Hours 9				
UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS					
19.	Flip flops – SR, JK, T, D,	1	T1,R6	202	T3,R6
20.	Master/Slave FF	1	R6,	219	T3,R6,R7
21.	operation and excitation tables, Triggering of FF,	1	R6	200	R6,R7
22.	Analysis and design of clocked sequential circuits	1	T1,R6	225	T3,R6
23.	Design - Moore/Mealy models,	1	T1	230	T3
24.	State minimization, state assignment,	1	R6	241	R6
25.	circuit implementation	1	R6	212	R6,R7
26.	Design of Counters- Ripple Counters,	1	R6	230	R6,R7
27.	Ring Counters, Shift registers, Universal Shift Register.	1	R6	243	R6,R7
	Total Hours 9				
UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS					
28.	Stable and Unstable states	1	T1,R5	202	BB
29.	output specifications,	1	T1,R6	219	BB
30	cycles and races,	1	R6	200	BB
31.	state reduction,	1	T1,R6	225	BB
32.	race free assignments,	1	T1	230	BB
33.	Hazards,	1	R6	241	BB
34.	Essential Hazards,	1	R6	212	BB
35.	Pulse mode sequential circuits,	1	R6	230	BB
36.	Design of Hazard free circuits.	1	R6	243	BB
	Total Hours 9				
UNIT V MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS					
37.	Basic memory structure – ROM -PROM EPROM – EEPROM –EAPROM, RAM	1	T1,R6	325	BB
38.	Static and dynamic RAM Programmable Logic Devices	1	R6	328	BB

39.	Programmable Logic Array (PLA) Programmable Array Logic (PAL)	1	T1,R6	331	BB
40.	Field Programmable Gate Arrays (FPGA)	1	T1,R6	335	BB
41.	Implementation of combinational logic circuits using PLA, PAL.	1	T1,R6	338	BB
42.	Digital integrated circuits: Logic levels, propagation delay,	1	T1,R6	340	BB
43.	power dissipation, fan-out and fanin,	1	T1,R6	343	BB
44.	noise margin, logic families and their characteristics	1	T1,R6	346	BB
45.	RTL, TTL, ECL, CMOS	1	T1	350	BB
Total Hours 9					
TOTAL HOURS = 45					

Content beyond the Syllabus

Introduction to HDL &VHDL